

CLAIMS

1. A method for reducing noise in the substrate of a chip, the method comprising:

- doping a substrate with a first dopant;
- doping a first well disposed on top of the substrate with a second dopant;
- doping a second well disposed within the first well with the second dopant;
- disposing a first transistor comprising at least one first transistor component within the second well, the first transistor adapted to employ a first type of channel having a quiet voltage source connected to a body thereof;
- disposing a third well doped with the first dopant within the first well; and
- disposing a second transistor comprising at least one second transistor component within the third well, the second transistor adapted to employ a second type of channel, the first well isolating noise between the second well and the substrate.

2. The method according to claim 1, further comprising coupling the first transistor and the second transistor in a complementary metal oxide semiconductor (CMOS) transistor arrangement.

3. The method according to claim 1, further comprising configuring the first transistor as a p-channel MOS (PMOS) transistor and the second transistor as an n-channel MOS (NMOS) transistor.

4. The method according to claim 3, further comprising coupling a noisy voltage source to a source of the PMOS transistor.

5. The method according to claim 4, further comprising the step of supplying approximately a same voltage level to the PMOS transistor using the noisy voltage source and the quiet voltage source provide.

6. The method according to claim 4, further comprising resistively coupling the body of the PMOS transistor to the second well.

7. The method according to claim 3, further comprising the step of coupling a body and a source of the NMOS transistor to a noisy voltage source.

8. The method according to claim 7, further comprising the step of capacitively coupling the body of the NMOS transistor to the substrate.

9. The method according to claim 3, wherein the step of doping the first well further comprises the step of doping a deep well disposed within the first well with the second dopant.

10. The method according to claim 3, further comprising the step of adapting the first well to shield the substrate from noise emanating from a voltage source coupled to at least one of the first transistor and the second transistor..

11. A method for reducing noise in a chip, the method comprising:
shielding a substrate layer of the chip from a transistor layer of the chip using a shielding layer;

capacitively coupling a p-type transistor within said transistor layer to said shielding layer, said p-type transistor having a quiet voltage source connected to a body thereof;

resistively coupling a n-type transistor within said transistor layer to said shielding layer; and

capacitively coupling said shielding layer to said substrate layer, said capacitively coupled shielding layer reducing the noise transferred to said substrate layer of the chip.

12. The method according to claim 11, wherein said shielding step further comprises disposing said shielding layer between said substrate layer and said transistor layer of the chip.

13. The method according to claim 11, wherein said shielding step further comprises the step of disposing a deep N-well, which represent said shielding layer, between said substrate layer and said transistor layer of the chip.

14. The method according to claim 11, further comprising the step of coupling a noisy voltage source to a source of said n-type transistor.

15. The method according to claim 14, further comprising the step of producing approximately the same voltage levels from said noisy voltage source and said quiet voltage source.

16. The method according to claim 13, further comprising the step of coupling a noisy voltage source to a source of said p-type transistor and a body of said p-type transistor.